



# BT-48 BERT/ParBERT



## DEVICE

### 16x3 Gb/s Parallel + 2 x 24 Gb/s Serial Bit Error Rate Test

## OVERVIEW

The Optilab BT48 is a cost effective bit error rate tester system. It consists of two benchtop units, BT3X16 and BT24X2. When used as a ParBERT, BT3X16 output 16 channels data pattern, and BT24X2 acts as the 16 channel error analyzer. The user selectable reference clock allows testing BER at a specific data rate with external clock input or at a pre-defined data rate using the internal clock. Each channel supports data rate up to 3 Gbps. Moreover, a SFI-5 compliant deskew channel provides parallel alignment information between channels. The error detector checks error rate in each data lane and detect channel parallel misalignment up to 15 UI. In addition to that, BT48 can be also configured to a dual channel 24 Gbps serial BERT by using BT24X2 as the pattern generator and BT3X16 as the error analyzer. An intuitive GUI, Optilab Teraport, is provided with the system for easy operation.

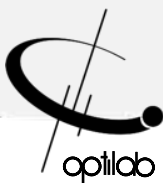
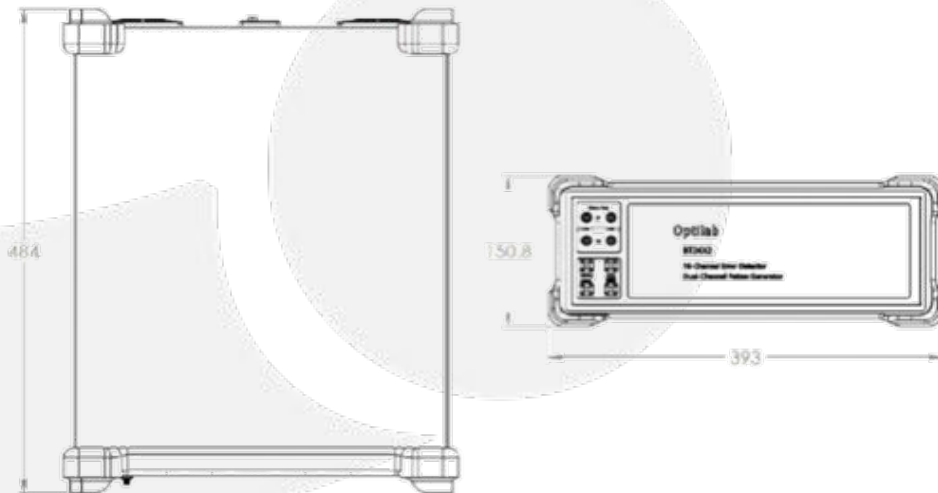
## FEATURES

- 16 Channel Synchronous In/Out
- Data Rates from 2.5 to 3.Gb/s per Channel
- Fixed Pattern or PRBS ( $2^7-1$  or  $2^{31}-1$ )
- Variable Delay up to 15 UI
- Error Injection Function
- Teraport GUI Software

## USE IN

- OC-768 MUX/DEMUX Testing
- SFI-4 and SFI-5
- SDH STM-256
- OTN OUT-3

## MECHANICAL DRAWING





# BT-48

## BERT/ParBERT

### PARALLEL PATTERN GENERATOR

Data Pattern	16 bit Flexed Pattern or PRBS (2 <sup>7</sup> -1 or 2 <sup>31</sup> -1)
Output Data Rate	2.5 Gb/s min, 3 Gb/s max
Output Data Amplitude	400 mVpp min, 800 mVpp max
Differential Output Impedance	100 Ω typ
Data Output FMS Jitter	5 ps typ
Rise/Falls Time (20% to 80%)	104 ps typ
Output Channel Delay Range	15 UI typ
Ref Clock Input Frequency	622.5 MHz min, 750 MHz max
Ref Clock Input Amplitude	-3 dBm min, 0 dBm typ, 5 dBm max
Monitor Clock Output Frequency	622.5 MHz min, 750 max

### PARALLEL ERROR DETECTOR

Data Pattern	16 bit Flexed Pattern or PRBS (2 <sup>7</sup> -1 or 2 <sup>31</sup> -1)
Input Data Rate	2.5 Gb/s min, 3 Gb/s max
Input Data Amplitude	100 mVpp min, 1000 mVpp max.
Differential Output Impedance	75 Ω min, 100 Ω typ, 125 Ω max
Ref Clock Input Frequency	622.5 MHz min, 750 MHz max
Ref Clock Input Amplitude	-3 dBm min, 0 dBm typ, 5 dBm max
Recovered Clock Frequency	622.5 MHz min, 750 max

### SERIAL PATTERN GENERATOR

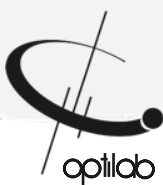
Data Pattern	128 bit Flexed Pattern or PRBS (2 <sup>7</sup> -1 or 2 <sup>31</sup> -1)
Output Data Rate	20 Gb/s min, 24 Gb/s max
Output Data Amplitude	100 mVpp min, 800 mVpp max.
Differential Output Impedance	100 Ω typ
Data Output RMS Jitter	1.9 ps typ
Rise/Fall Time (20% to 80%)	20 ps typ

### SERIAL ERROR DETECTOR

Data Pattern	128 bit Flexed Pattern or PRBS (2 <sup>7</sup> -1 or 2 <sup>31</sup> -1)
Input Data Rate	20 Gb/s min, 24 Gb/s max
Input Data Amplitude	100 mVpp min, 800 mVpp max.
Differential Output Impedance	100 Ω typ
Lock Mode	Lock to ref clock or lock to data

### SYSTEM SPECIFICATION

Operating Temperature	-20 °C to +85 °C
Storage Temperature	-5 °C to +50 °C
Data Electrical Connectors (Parallel)	SMA Female, AC Coupled, Differential
Data Electrical Connectors (Serial)	SMA Female, DC Coupled, Differential
Power Supply Requirements	100 - 240 VAC
Dimensions	Two benchtop units, each 484 x 393 x 151 (mm)





# BT-48

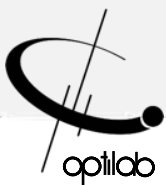
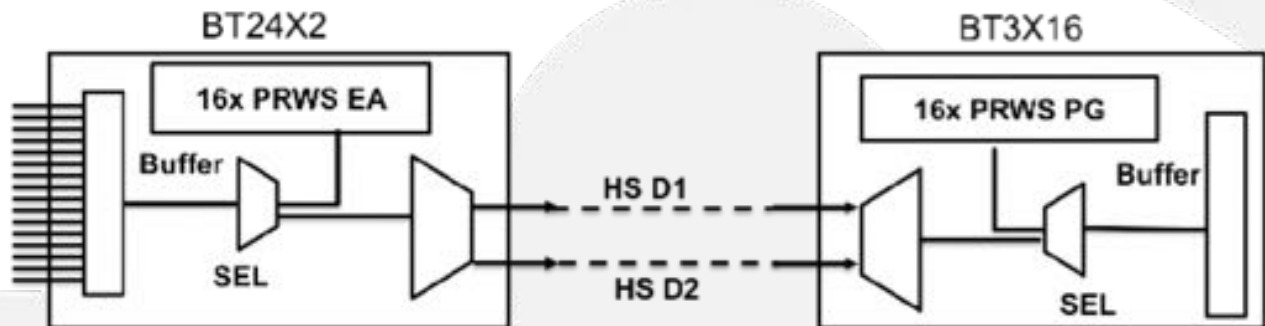
## BERT/ParBERT

### APPLICATION DIAGRAMS

#### 16X CHANNEL 3 GB/S PARBERT CONFIGURATION



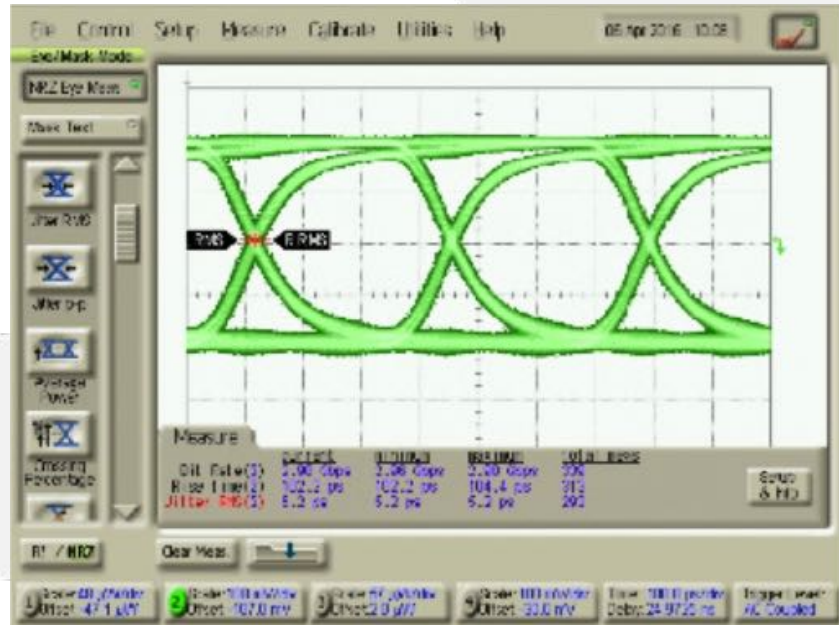
#### 2X CHANNEL 24 GB/S SERIAL BERT CONFIGURATION



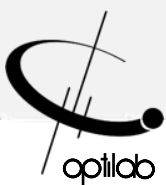
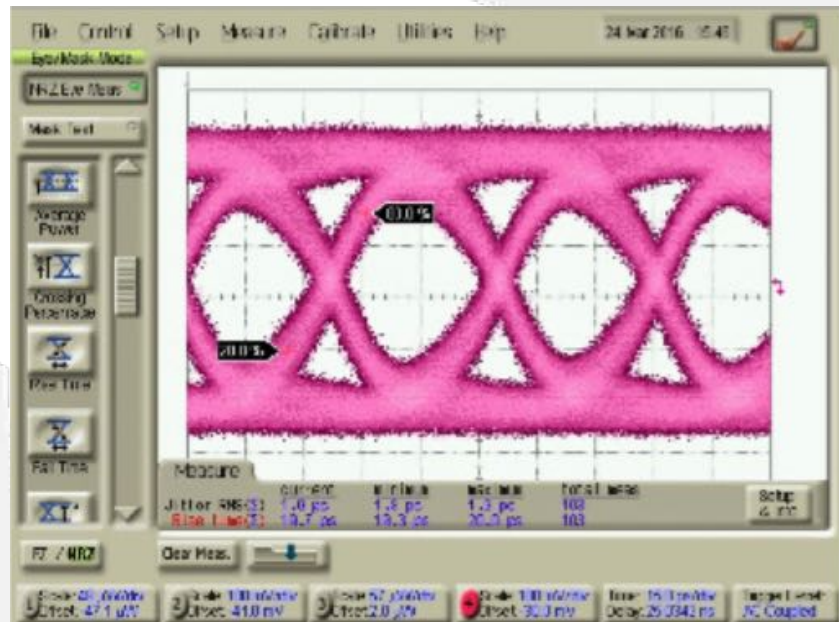


# BT-48 BERT/ParBERT

EYE DIAGRAM 3 GB/S DATA



EYE DIAGRAM 24 GB/S DATA





# BT-48 BERT/ParBERT

TERAPORT  
GUI SOFTWARE

Optilab **Teraport** 16-Channel Parallel BERT System

Configure Error Checker

Cycles to Check: 0

PRBS Pattern: 2<sup>31</sup>

Run EC Self Test

EC Feedback

EC Overflow

Cycles Checked: 0

	Error Count	BER	Lock Status
P	0	0	
0	0	0	
1	0	0	
2	0	0	
3	0	0	
4	0	0	
5	0	0	
6	0	0	
7	0	0	
8	0	0	
9	0	0	
10	0	0	
11	0	0	
12	0	0	
13	0	0	
14	0	0	
15	0	0	

Status

- CMU Lock
- Frame Lock
- TXOOA

FIFO Full Empty TXOOA Skew

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	D
Full																	
Empty																	
TXOOA																	
Skew	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

V1.0.0

Optilab **Teraport JUPITER**

2-Channel Bit Error Rate Tester (BERT)

Configuration

BERT Configuration

Cycles to Check: 400568256

PRBS Pattern: 2<sup>31</sup>

Self Test

Test Iterations (Multiple mode only): 0

Test Mode: Single Multiple Continuous

Run EC Test

Error Checking

- Error Check Disabled
- EC Overflow

Multiple Test Iterations Mode: Run # 1

Cycles Checked: 0

	Error Count	BER
P	0	0
Ch. 1	0	0
Ch. 2	0	0

BER

Clear Chart Save Data

Iterations

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